We claim:

1. A power amplifier for receiving a first input signal at a first input terminal and for producing a first output signal at a first output terminal, said first output signal corresponding to said first input signal, a first signal amplifier being coupled to the input terminal to receive the input signal and coupled to the output terminal to provide the output signal, the first signal amplifier having a first power terminal for receiving a total power signal and said power amplifier having a first power supply circuit comprising:

(a) a first input signal compensation block coupled to the first input terminal to receive the first input signal and to provide a compensated input signal corresponding to the first input signal, wherein the compensated input signal defines a target power level;

(b) a power signal compensation block for receiving the total power signal and for providing a compensated power signal corresponding to the total power signal;

(c) a summer coupled to the input signal compensation block and to the power signal compensation block for providing an error signal corresponding to a difference between the target power level and the power level of the total power signal;

(d) a control circuit coupled to the summer for receiving the error signal and for providing a first control signal and a second control signal in response to the error signal, wherein the first control signal corresponds to a target main power signal level and the second control signal corresponds to a target transient power signal level;

(e) a transient detect block coupled to the input signal compensation block for providing a transient signal to identify a transient condition when the rate of change in the slew rate of the compensated input signal exceeds a selected transient threshold;

(f) a main power supply for providing a main power signal at the first power terminal in response to the first control signal; and

(g) a selectively engageable transient power supply for providing a transient power signal at the first power terminal in response to the second control signal and the transient signal, wherein the transient power supply is engaged when the transient signal indicates that a transient condition exists;

wherein the control circuit provides the first and second control signals such that the target main power signal level is equal to or higher than the target transient power signal level and wherein the magnitude of the total power signal is generally equal to the higher of the magnitude of the main power signal or the magnitude of the transient power signal.

2. The power amplifier of claim 1 wherein the first input compensation circuit includes:

(i) an offset block for adding an offset to said input signal to provide an offset input signal;

(ii) a frequency compensation block for receiving the offset input signal and for providing a corresponding frequency compensated circuit having its voltage components phase advanced with respect to its current component; and

(iii) a first rectifier for rectifying the frequency compensated circuit to provide the compensated input signal.

3. The power amplifier of claim 2 wherein the frequency compensation block is configured to amplify the amplitude of selected the frequency compensated signal at selected frequency components, wherein said selected frequency components exceed a selected frequency compensation threshold.

4. The power amplifier of claim 3 wherein the amplitude of the selected frequency components is progressively amplified to a greater extent.

5. The power amplifier of claim 3 wherein the amplitude of the selected frequency components is equally amplified.

6. The power amplifier of claim 2 wherein the first rectifier is a half wave rectifier.

7. The power amplifier of claim 2 wherein the input offset block is configured to add a smaller offset to the first input signal if the highest frequency component of the input signal is less than a selected offset frequency threshold and to add a larger offset to the first input signal otherwise.

8. The power amplifier of claim 1 wherein the first input compensation block provides the compensated input signal corresponding to a target power level that exceeds the sum of the power required by the first amplifier to generate a first output signal corresponding to the first input signal and at least half of a ripple in the main power signal.

9. The power amplifier of claim 1 wherein the first control circuit is a PWM signal having a fixed switching frequency.

10. The power amplifier of claim 9 wherein the main power supply is a switching regulator including:

(i) a main power source;

(ii) a switch coupled to the power source and responsive to the first control signal to provide an unfiltered main power signal; and

(ii) an integrating filter coupled to switch to provide the main power signal corresponding to the unfiltered power signal.

11. The power amplifier of claim 10 wherein the switching frequency is selected to limit the EMI emitted by the main power supply to a selected maximum EMI limit.

12. The power supply of claim 10 wherein the transient detect block includes:

(i) a peak detector for providing a peak signal corresponding to the peak envelope of the compensated input signal;

(ii) a differentiator coupled to the peak detector for providing a differentiated signal corresponding to the rate of change of the compensated input signal; and

(iii) a comparator for comparing the differentiated signal with the transient threshold to provide the transient signal;

and wherein the transient power supply includes:

(iv) a transient power source;

(v) a transient power regulator coupled to the control circuit for receiving the second control signal; and

(iv) a transient supply switch for engaging the transient power regulator in response to the transient signal.

13. The power amplifier of claim 12 wherein the main power source and transient power source are the same.

14. The power amplifier of claim 12 wherein the transient power regulator is a linear regulator.

15. The power amplifier of claim 14 wherein the transient power regulator includes a MOSFET.

16. The power amplifier of claim 11 wherein a time constant of the integrating filter is selected to effectively smooth the main power signal compared to the unfiltered power signal.

17. The power amplifier of claim 12 wherein a discharge rate of the peak detector is selected to correspond to a slew rate of the main power supply.

18. The power amplifier of claim 1 further including:

(i) an overload detect block coupled to the first signal amplifier to provide an overload signal corresponding to one or more overload conditions within the first signal amplifier; and

(ii) means for combining the overload signal with the compensated input signal to provide an adjusted compensated input signal;

wherein the error signal corresponds to a difference between the adjusted compensated input signal and the compensated power signal.

19. The power amplifier of claim 18 wherein the means for combining is the summer.

20. The power amplifier of claim 18 wherein the means for combining is a second summer.

21. The power amplifier of claim 1 wherein a second signal amplifier is coupled to the first power terminal and a second input signal is received at a second input terminal and wherein the first input signal compensation block provides a first compensated input signal and further including:

(i) a second input signal compensation for providing a second compensated input signal; and

(ii) a combining circuit for combining the first and second compensated input signals to provide the compensated input signal having a magnitude corresponding to the higher magnitude of the first and second compensated input signals.

22. The power amplifier of claim 21 wherein the combining circuit is a pair of diodes for diode OR'ing the first and second compensated input signals.

23. The power amplifier of claim 2 wherein the first control signal is a pulse density modulated control signal and wherein the main power supply is a resonant switching power regulator.

24. The power amplifier of claim 23 wherein the main power supply is a zero-current switching regulator and includes a LC resonant tank.

25. The power amplifier of claim 1 further including a low voltage power supply coupled for providing a fixed low voltage power signal to the first power terminal, wherein the total power signal is generally equal to the higher of the magnitude of the main power signal, the magnitude of the transient power signal or the magnitude of the low voltage power signal.

26. The power amplifier of claim 25 wherein the control circuit is configured to set the main power signal to zero when the target power level is less than the magnitude of the low voltage power signal.

27. The power amplifier of claim 23 further including a post regulation circuit having:

(i) an overload detect block coupled to the first signal amplifier to provide an overload signal corresponding to one or more overload conditions within the first signal amplifier;

(ii) a second rectifier coupled to the offset block for receiving the offset input signal and providing a rectified input signal;

(iii) a third summer for subtracting the overload signal from the rectified input signal to provide a regulation signal;

(iv) a regulation amplifier coupled to the third summer for providing a amplified regulation signal corresponding to the regulation signal and having a magnitude range corresponding to the magnitude range of the total power signal;

(v) a post regulator having a control terminal, and coupled between the main and transient power supplies and the first power terminal; and

(vi) a regulation feedback circuit coupled between the first power terminal and the control terminal of the post regulator and including a fourth

summer for providing a regulator error signal corresponding to the difference between the total power signal and the amplified regulation signal;

wherein the post regulator regulates the total power signal in response to the regulator error signal when an overload condition occurs.

28. The power amplifier of any one of claims 2-5 or 7-27 wherein the first amplifier is a bridge amplifier and wherein the first rectifier is a full wave rectifier.

29. The power amplifier of any of claims 1-27 wherein the first signal amplifier has a second power terminal and further including a second power supply circuit having the same structure as said first power supply circuit, wherein said first power supply circuit supplies power to said first signal amplifier at said first power terminal during positive half wave of said output signal and said second power supply circuit provides power to said first signal amplifier at said second power terminal during negative half waves of said output signal.

30. The power amplifier of claim 1 further including an EMI isolation circuit coupled between said first input terminal and an internal input terminal for providing a first EMI-decoupled signal corresponding to said first input signal at said internal input terminal, and wherein said first input signal compensation block and said first signal amplifier are coupled to said internal input node, wherein the EMI isolation circuit has:

(i) a first isolation amplifier having a first amplification factor coupled to said first input terminal through a first impedance for receiving said input signal and for providing an amplified input signal; and

(ii) a second isolation amplifier having a second amplification factor coupled to said first amplifier for receiving said amplified input signal and to said internal input terminal for providing said first EMI-decoupled signal;

wherein the amplification factor of the first isolation amplifier is greater than 1 and the amplification factor of said second isolation amplifier is less than 1.

31. The power amplifier of claim 30 wherein said first impedance is greater than 50 kΩ.

32. The power amplifier of claim 30 wherein said first impedance is equal to or greater than 100 kΩ.

33. The power amplifier of claim 30 wherein the EMI isolation circuit further has an EMI shield for encompassing the first and second isolation amplifiers and the first power supply circuit.

34. A power amplifier for receiving a first input signal at a first input terminal and for producing a first output signal at a first output terminal, said first output signal corresponding to said first input signal, a first signal amplifier being coupled to the input terminal to receive the input signal and coupled to the output terminal to provide the output signal, the first signal amplifier having a first power terminal for receiving a total power signal and said power amplifier having a first power supply circuit comprising:

(a) a first input signal compensation block coupled to the first input terminal to receive the first input signal and to provide a compensated input signal corresponding to the first input signal, wherein the compensated input signal defines a target power level;

(b) a power signal compensation block for receiving the total power signal and for providing a compensated power signal corresponding to the total power signal;

(c) a summer coupled to the input signal compensation block and to the power signal compensation block for providing an error signal corresponding to a difference between the target power level and the power level of the total power signal;

(d) a transient detect block coupled to the input signal compensation block for providing a transient signal to identify a transient condition when the rate of change in the slew rate of the compensated input signal exceeds a selected transient threshold;

(e) a first transient control circuit coupled to the transient detect block for providing first and second digital transient control signals, wherein the first transient control signal indicates the occurrence of a transient condition for a first time period in response to the transient signal and wherein the second transient control signal indicates the occurrence of a transient condition for a second time period in response to the transient signal, and wherein the second time period is longer than the first time period;

(f) a control circuit coupled to the summer for receiving an amplified error signal for providing a first control signal in response to the amplified error signal;

(g) a signal combining block for combining the first control signal and the first transient control signal to provide a main power supply control signal;

(h) a selectively engageable second transient control circuit coupled to the first transient control signal for receiving the second transient control circuit and for temporarily increasing the magnitude of the error signal, wherein the second transient control circuit is engaged and disengaged in response to the second transient control signal, the second transient control circuit including a feedback amplifier coupled between the summer and the control circuit to provide the amplified error signal, the feedback amplifier being operative at all times; and

(i) a main power supply for providing a main power signal at the first power terminal in response to the main power supply control signal;

wherein the total power signal corresponds to the main power signal.

35. The power supply circuit of claim 34 wherein the first transient control circuit includes a first one-shot circuit for generating the first transient control signal, wherein the first one-shot circuit is triggered by the transient signal indicating the occurrence of a transient condition.

36. The power supply circuit of claim 35 wherein the first transient control circuit includes a second one-shot circuit for generating the second transient control signal, wherein the second one-shot is triggered by the transient signal indicating the occurrence of a transient condition.

37. The power supply circuit of claim 36 wherein the second transient control circuit includes:

(i) a fast release block for initially increasing the error signal rapidly when the second transient control circuit becomes engaged; and

(ii) a slow release block for slowly reducing the increase in the error signal.

38. The power supply circuit of claim 37 wherein the first time period is selected to be longer than the time required for the fast attack block to increase the magnitude of the error signal.

39. The power supply circuit of claim 37 wherein the second transient control circuit comprises:

(i) a first diode having its cathode coupled to the output of the second one-shot circuit and having its anode coupled to first node;

(ii) a first capacitor coupled between the first node and ground;

(iii) a first resistor and a second capacitor coupled in parallel between the first node and a second node, wherein the second node is coupled to a third node at the coupling of the summer and the power signal compensation block; and

(iv) a feedback network including a second resistor and a third capacitor coupled between the third node and a fourth node at the coupling of the feedback amplifier and the control circuit.

40. The power supply circuit of claim 39 wherein:

(i) the second transient control signal is normally high in the absence of a transient condition and becomes low when the second one-shot is triggered;

(ii) the first capacitor is normally charged in the absence of a transient condition and is discharged through the first diode when the second one-shot is triggered; and

(iii) the first and second resistances act as a voltage divider in response to the discharging of the first capacitor to initially increase the magnitude of the amplified error signal.

41. The power supply circuit of claim 37 wherein the signal combining block includes an OR gate.

42. The power supply circuit of claim 39 wherein the first input compensation circuit includes:

(i) an offset block for adding an offset to said input signal to provide an offset input signal;

(ii) a frequency compensation block for receiving the offset input signal and for providing a corresponding frequency compensated circuit having its voltage components phase advanced with respect to its current component; and

(iii) a first rectifier for rectifying the frequency compensated circuit to provide the compensated input signal.

43. The power supply circuit of claim 42 wherein the frequency compensation block is configured to amplify the amplitude of selected the frequency compensated signal

at selected frequency components, wherein said selected frequencies exceed a selected frequency compensation threshold.

44. The power supply circuit of claim 43 wherein the amplitude of the selected frequency components is progressively amplified to a greater extent.

45. The power supply circuit of claim 43 wherein the amplitude of the selected frequency components is equally amplified.

46. The power supply circuit of claim 42 wherein the first rectifier is a half wave rectifier.

47. The power supply circuit of claim 42 wherein the input offset block is configured to add a smaller offset to the first input signal if the highest frequency component of the input signal is less than a selected offset frequency threshold and to add a larger offset to the first input signal otherwise.

48. The power supply circuit of claim 42 wherein the first input compensation block provides the compensated input signal corresponding to a target power level that exceeds the sum of the power required by the first amplifier to generate a first output signal corresponding to the first input signal and at least half of a ripple in the main power signal.

49. The power supply circuit of claim 40 wherein the first control circuit is a PWM signal having a fixed switching frequency.

50. The power supply circuit of claim 39 wherein the main power supply is a switching regulator including:

(i) a main power source;

(ii) a switch coupled to the power source and responsive to the first control signal to provide an unfiltered main power signal; and

(iii) an integrating filter coupled to switch to provide the main power signal corresponding to the unfiltered power signal.

51. The power supply circuit of claim 50 wherein the switching frequency is selected to limit the EMI emitted by the main power supply to a selected maximum EMI limit.

52. The power supply of claim 50 wherein the transient detect block includes:

(i) a peak detector for providing a peak signal corresponding to the peak envelope of the compensated input signal;

(ii) a differentiator coupled to the peak detector for providing a differentiated signal corresponding to the rate of change of the compensated input signal; and

(iii) a comparator for comparing the differentiated signal with the transient threshold to provide the transient signal.

53. The power supply circuit of claim 51 wherein a time constant of the integrating filter is selected to effectively smooth the main power signal compared to the unfiltered power signal.

54. The power supply circuit of claim 52 wherein a discharge rate of the peak detector is selected to correspond to a slew rate of the main power supply.

55. The power supply circuit of claim 40 further including:

(i) an overload detect block coupled to the first amplifier to provide an overload signal corresponding to one or more overload conditions within the first amplifier; and

(ii) means for combining the overload signal with the compensated input signal to provide an adjusted compensated input signal;

wherein the error signal corresponds to the adjusted compensated input signal and compensated power signal.

56. The power supply circuit of claim 55 wherein the means for combining is the summer.

57. The power supply circuit of claim 55 wherein the means for combining is a second summer.

58. The power supply circuit of claim 40 wherein a second amplifier is coupled to the power terminal and a second input signal is received at a second input terminal and wherein the first input signal compensation block provides a first compensated input signal and further including:

(i) a second input signal compensation from for providing a second compensated input signal; and

(ii) a combining circuit for combining the first and second compensated input signals to provide the compensated input signal having a magnitude corresponding to the higher of the first and second compensated input signals.

59. The power supply circuit of claim 58 wherein the combining circuit is a pair of diodes for diode OR'ing the first and second compensated input signals.

60. The power supply circuit of claim 40 wherein the first control signal is a pulse density modulated control signal and wherein the main power supply is a resonant switching power regulator.

61. The power supply circuit of claim 60 wherein the main power supply is a zero-current switching regulator and includes a LC resonant tank.

62. The power supply circuit of claim 40 further including a low voltage power supply coupled for providing a fixed low voltage power signal to the power terminal, wherein the total power signal is generally equal to the higher of the magnitude of the

main power signal, the magnitude of the transient power signal or the magnitude of the low voltage power signal.

63. The power supply circuit of claim 62 wherein the control circuit is configured to set the main power signal to zero when the target power level is less than the magnitude of the low voltage power signal.

64. The power supply circuit of claim 60 further including a post regulation circuit having:

(i) an overload detect block coupled to the first amplifier to provide an overload signal corresponding to one or more overload conditions within the first amplifier;

(ii) a second rectifier coupled to the offset block for receiving the offset input signal and providing a rectified input signal;

(iii) a third summer for subtracting the overload signal from the rectified input signal to provide a regulation signal;

(iv) a regulation amplifier coupled to the third summer for providing a amplified regulation signal corresponding to the regulation signal and having a magnitude range corresponding to the magnitude range of the total power signal;

(v) a post regulator having a control terminal, and coupled between the main and transient power supplies and the power terminal; and

(vi) a regulation feedback circuit coupled between the power terminal and the control terminal of the post regulator and including a fourth summer for providing a regulator error signal corresponding to the difference between the total power signal and the amplified regulation signal;

wherein the post regulator regulates the total power signal in response to the regulator error signal when an overload condition occurs.

65. The power supply circuit of any one of claims 40-45 or 47-64 wherein the first amplifier is a bridge amplifier and wherein the first rectifier is a full wave rectifier.

66. The power amplifier of any of claims 40-64 wherein the first signal amplifier has a second power terminal and further including a second power supply circuit having the same structure as said first power supply circuit, wherein said first power supply circuit supplies power to said first signal amplifier at said first power terminal during positive half wave of said output signal and said second power supply circuit provides power to said first signal amplifier at said second power terminal during negative half waves of said output signal.

67. The power amplifier of claim 34 further including an EMI isolation circuit coupled between said first input terminal and an internal input terminal for providing a first EMI-decoupled signal corresponding to said first input signal at said internal input terminal, and wherein said first input signal compensation block and said first signal amplifier are coupled to said internal input node, wherein the EMI isolation circuit has:

(i) a first isolation amplifier having a first amplification factor coupled to said first input terminal through a first impedance for receiving said input signal and for providing an amplified input signal; and

(ii) a second isolation amplifier having a second amplification factor coupled to said first amplifier for receiving said amplified input signal and to said internal input terminal for providing said first EMI-decoupled signal;

wherein the amplification factor of the first isolation amplifier is greater than 1 and the amplification factor of said second isolation amplifier is less than 1.

68. The power amplifier of claim 64 wherein said first impedance is greater than 50 kΩ.

69. The power amplifier of claim 64 wherein said first impedance is equal to or greater than 100 kΩ.

70. A method of supplying a total power signal to a signal amplifier, comprising:

(a) receiving an input signal;

(b) producing a compensated input signal corresponding to the input signal, the compensated input signal defining a target power level for the power signal;

(c) comparing the compensated signal to a reduced version of the power signal to produce an error signal;

(d) providing first and second control signals in response to the error signal;

(e) providing a main power signal using a switching regulator in response to the first control signal, the main power signal being a first part of the total power signal;

(f) comparing the rate of change of the compensated input signal to a selected transient threshold to provide a transient signal, the transient signal identifying a transient condition when the rate of change exceeds the threshold, the transient threshold corresponding to the maximum slew rate of the main power supply; and

(g) engaging a transient power supply to provide a transient power signal in response to said second control signal, when the transient signal indicates a transient condition, the transient power signal being a second part of the total power signal.

71. The method of claim 70 wherein step (b) includes:

(i) adding an offset the input signal;

(ii) amplifying frequency components of the input signal exceeding a selected threshold frequency; and

(iii) rectifying the result of step (b).

72. The method of claim 71 wherein step (i) is performed after step (iii).

73. The method of claim 71 wherein step (i) is performed by adding a smaller offset to frequency components below a selected threshold and adding a larger offset to frequency components above the threshold.

74. The method of claim 70 wherein step (f) is performed by:

(i) peak detecting the compensated input signal;

(ii) differentiating the result of step (i); and

(iii) comparing the result of step (ii) with the transient threshold.

75. The method of claim 74 wherein a discharge rate of the peak detector is selected to correspond to the slew rate of the main power signal.

76. The method of claim 70 further including providing an overload signal corresponding to an overload condition in the amplifier and reducing the magnitude of the main power signal in response to the overload signal.

77. The method of claim 70 wherein the first control signal is a PWM signal.

78. The method of claim 70 wherein the switching regulator is a resonant switching power regulator, and wherein the first control signal is a PDM signal.

79. The method of claim 70 further including providing a low voltage DC power signal as a third part of the total power signal.

80. The method of claim 79 further including disabling the switching regulator when the target power level is less than the magnitude of the low voltage DC power signal.

81. The method of claim 70 further including regulating the total power signal using a post regulator.

82. The method of claim 81 further including providing an overload signal corresponding to an overload condition in the amplifier and reducing the magnitude of the total power signal in response to the overload signal.

83. The method of claim 71 wherein the amplifier is a bridge amplifier and step (iii) is performed by full wave rectifying the result of step (ii).

84. A method of supplying a total power signal to a signal amplifier, comprising:

(a) receiving an input signal;

(b) producing a compensated input signal corresponding to the input signal, the compensated input signal defining a target power level for the power signal;

(c) comparing the compensated signal to a reduced version of the power signal to produce an error signal;

(d) providing first and second control signals in response to the error signal;

(e) providing a main power signal using a switching regulator in response to the first control signal, the main power signal being a first part of the total power signal;

(f) comparing the rate of change of the compensated input signal to a selected transient threshold to provide a transient signal, the transient signal identifying a transient condition when the rate of change exceeds the threshold, the transient threshold corresponding to the maximum slew rate of the main power supply; and

(g) in response to a transient condition, temporarily engaging the switching regulator with a 100% duty cycle for a first time period and temporarily elevating the error signal for a second time period.

85. The method of claim 84 wherein step (b) includes:

(i) adding an offset the input signal;

(ii) amplifying frequency components of the input signal exceeding a selected threshold frequency; and

(iii) rectifying the result of step (b).

86. The method of claim 85 wherein step (i) is performed after step (iii).

87. The method of claim 85 wherein step (i) is performed by adding a smaller offset to frequency components below a selected threshold and adding a larger offset to frequency components above the threshold.

88. The method of claim 84 wherein step (f) is performed by:

(i) peak detecting the compensated input signal;

(ii) differentiating the result of step (i); and

(iii) comparing the result of step (ii) with the transient threshold.

89. The method of claim 88 wherein a discharge rate of the peak detector is selected to correspond to the slew rate of the main power signal.

90. The method of claim 84 further including providing an overload signal corresponding to an overload condition in the amplifier and reducing the magnitude of the main power signal in response to the overload signal.

91. The method of claim 84 wherein the first control signal is a PWM signal.

92. The method of claim 84 wherein the switching regulator is a resonant switching power regulator, and wherein the first control signal is a PDM signal.

93. The method of claim 84 further including providing a low voltage DC power signal as a second part of the total power signal.

94. The method of claim 93 further including disabling the switching regulator when the target power level is less than the magnitude of the low voltage DC power signal.

95. The method of claim 84 further including regulating the total power signal using a post regulator.

96. The method of claim 95 further including providing an overload signal corresponding to an overload condition in the amplifier and reducing the magnitude of the total power signal in response to the overload signal.

97. The method of claim 85 wherein the amplifier is a bridge amplifier and step (iii) is performed by full wave rectifying the result of step (ii).

98. A power amplifier for receiving a first input signal at a first input terminal and for producing a first output signal at a first output terminal, said first output signal corresponding to said first input signal, a first signal amplifier being coupled to the input terminal to receive the input signal and coupled to the output terminal to provide the output signal, the first signal amplifier having a first power terminal for receiving a total power signal and said power amplifier having a first power supply circuit comprising:

(a) a first input signal compensation block coupled to the first input terminal to receive the first input signal and to provide a compensated input signal corresponding to the first input signal, wherein the compensated input signal defines a target power level;

(b) a main power signal compensation block for receiving a main power signal and for providing a compensated main power signal corresponding to the main power signal;

(c) a first summer coupled to the input signal compensation block and to the main power signal compensation block for providing a first error signal corresponding to a difference between the target power level and the power level of the main power signal;

(d) a first control circuit coupled to the summer for receiving the first error signal and for providing a first control signal in response to the second

error signal, wherein the first control signal corresponds to a target main power signal level;

(e) a total power signal compensation block for receiving the total power signal and for providing a compensated total power signal corresponding to the total power signal;

(f) a second summer coupled to the input signal compensation block and to the total power signal compensation block for providing a second error signal corresponding to a difference between the target power level and the power level of the total power signal;

(g) a second control circuit coupled to the summer for receiving the second error signal and for providing a second control signal in response to the second error signal, wherein the second control signal corresponds to a target transient power signal level;

(h) a transient detect block coupled to the input signal compensation block for providing a transient signal to identify a transient condition when the rate of change in the slew rate of the compensated input signal exceeds a selected transient threshold;

(i) a main power supply for providing a main power signal at the first power terminal in response to the first control signal; and

(j) a selectively engageable transient power supply for providing a transient power signal at the first power terminal in response to the second control signal and the transient signal, wherein the transient power supply is engaged when the transient signal indicates that a transient condition exists;

wherein the magnitude of the total power signal is generally equal to the higher of the magnitude of the main power signal or the magnitude of the transient power signal.